CLAIMS

What is claimed is:

1. A memory array comprising:

a) a multiplicity of row conductors and a multiplicity of column conductors, the row conductors and column conductors being arranged to cross at cross-points, and

b) a memory cell disposed at each cross-point, each memory cell having a storage element and a control element coupled in series between a row conductor and a column conductor, and each control element including a silicon-rich insulator.

2. The memory array of claim 1, wherein the silicon-rich insulator of each memory cell is patterned.

3. The memory array of claim 1, wherein the silicon-rich insulator of each memory cell comprises silicon-rich oxide (SRO).

4. The memory array of claim 1, wherein the silicon-rich insulator of each memory cell is electrically isolated from the silicon-rich insulators of all other memory cells.

5. The memory array of claim 1, wherein the control element of each memory cell further comprises a tunnel junction.

6. The memory array of claim 1, wherein the storage element of each memory cell comprises an anti-fuse.

7. The memory array of claim 1, wherein the storage element of each memory cell comprises a fuse.

8. The memory array of claim 1, wherein the storage element of each memory cell comprises a tunnel junction.

9. The memory array of claim 1, wherein the storage element of each memory cell comprises a state-change layer.

10. The memory array of claim 9, wherein the state-change layer of the storage element comprises a chalcogenide.

11. The memory array of claim 1, wherein the row conductors are arranged in mutually orthogonal relationship with the column conductors.

12. A memory array comprising:

a) a multiplicity of row conductors and a multiplicity of column conductors, the row conductors and column conductors arranged to cross at cross-points, and

b) a memory cell disposed at each cross-point, each memory cell having a storage element and a control element coupled in series between a row conductor and a column conductor,

each storage element comprising a tunnel-junction anti-fuse, and

each control element comprising a patterned silicon-rich insulator and a tunnel junction.

13. A memory cell comprising:

a storage element comprising a tunnel-junction anti-fuse, and

a control element coupled in series with the storage element, the control element comprising a patterned silicon-rich insulator and a tunnel junction.

14. The memory cell of claim 13, wherein the patterned silicon-rich insulator of the control element injects current into the tunnel junction of the control element when the memory cell is selected and isolates the storage element when the memory cell is unselected.

15. A memory array comprising:

a multiplicity of row conductors and a multiplicity of column conductors, the row conductors and column conductors arranged to cross at cross-points, and

the memory cell of claim 13 disposed at each cross-point.

16. A memory array comprising:

a) a multiplicity of row conductors and a multiplicity of column conductors, the row conductors and column conductors being arranged to cross at cross-points, and

b) a memory cell disposed at each cross-point, each memory cell comprising means for storing data and means for controlling the means for storing data, the means for storing data and means for controlling being coupled in series between a row conductor and a column conductor, and each means for controlling including a silicon-rich insulator.

17. A method for controlling a memory cell of the type having an anti-fuse storage element, the method comprising the steps of:

a) providing a patterned silicon-rich insulator combined with a tunnel junction to form a control element, whereby the memory cell is isolated when unselected,

b) coupling the control element in series with the anti-fuse storage element, and

c) providing conductive elements for supplying current to selectively inject current from the silicon-rich insulator into the tunnel junction of the control element when selecting the memory cell.

18. A memory cell controlled in accordance with the method of claim 17.

19. A memory array comprising:

a multiplicity of row conductors and a multiplicity of column conductors, the row conductors and column conductors arranged to cross at cross-points, and

the memory cell of claim 18 disposed at each cross-point.

20. A method for fabricating a memory cell, the method comprising the steps of:

a) providing a substrate,

b) depositing and patterning a first conductive layer over the substrate,

c) forming a storage layer,

d) forming a layer of silicon-rich insulator,

e) forming a tunnel-junction layer over the layer of silicon-rich insulator, and

f) forming and patterning a second conductive layer over the tunnel-junction layer.

21. The method of claim 20, further comprising the step of patterning the layer of silicon-rich insulator.

22. The method of claim 20, further comprising the step of depositing an interlayer dielectric (ILD).

23. The method of claim 22, further comprising the step of planarizing the interlayer dielectric (ILD).

24. The method of claim 20, further comprising the step of forming a conductive electrode disposed contiguous with the layer of silicon-rich insulator.

25. The method of claim 24, further comprising the step of patterning the conductive electrode.

26. A memory cell made by the method of claim 20.

27. A memory array comprising a multiplicity of the memory cells of claim 26.

28. A substrate carrying electronics comprising the memory array of claim 27.

29. An integrated circuit comprising the memory array of claim 27.

30. A multilayer memory comprising:

a) a multiplicity of the memory arrays of claim 27, arranged in memory layers,

b) a multiplicity of interlayer dielectrics disposed to separate adjacent memory layers, and

c) conductive vias selectively extending through the interlayer dielectrics to selectively interconnect memory cells of the memory arrays.

31. A substrate carrying electronics comprising the multilayer memory of claim 30.

32. An integrated circuit comprising the multilayer memory of claim 30.

33. The multilayer memory of claim 30, wherein the memory cells of the multilayer memory are organized in sets, the memory cells of each set being at least partially aligned vertically with each other.

34. The multilayer memory of claim 33, wherein conductive vias interconnecting memory cells of each set are interconnected electrically to form a common node for that set of memory cells.

35. The multilayer memory of claim 34, wherein the conductive vias interconnecting memory cells of each set are at least partially aligned vertically.

36. A method for fabricating a multilayer memory, the method comprising the steps of:

i) performing the steps of claim 20 to form a first memory layer,

ii) depositing an interlayer dielectric, whereby a substrate for a subsequent memory layer is formed,

iii) performing steps b) through f) of claim 20, and

iv) repeating steps ii) and iii) until a desired number of memory layers is formed.

37. The method of claim 20, further comprising the steps of:

g) forming and patterning an interlayer dielectric over the storage layer,

h) forming an opening through the interlayer dielectric and extending to the storage layer, and

i) filling the opening through the interlayer dielectric with conductive material to form a middle electrode contiguous with the storage layer.

38. A memory cell made by the method of claim 37.

39. A memory array comprising a multiplicity of the memory cells of claim 38.

40. A substrate carrying electronics comprising the memory array of claim 39.

41. An integrated circuit comprising the memory array of claim 39.

42. A method for fabricating a multilayer memory, the method comprising the steps of:

a) providing a substrate,

b) depositing and patterning a first conductive layer over the substrate,

c) forming a storage layer,

d) forming and patterning a first interlayer dielectric over the storage layer,

e) forming an opening through the first interlayer dielectric and extending to the storage layer,

f) filling the opening through the first interlayer dielectric with conductive material to form a middle electrode,

g) forming a layer of silicon-rich insulator, at least a portion of the silicon-rich insulator being disposed contiguous with the middle electrode,

h) forming a tunnel-junction layer over the layer of silicon-rich insulator,

i) forming and patterning a second conductive layer over the tunnel-junction layer and at least partially aligned with the middle electrode,

j) forming and patterning a second interlayer dielectric, whereby a substrate is formed for subsequent layers,

k) forming vias as required through the second interlayer dielectric, and

l) repeating steps b) through k) until a desired number of memory array layers have been formed.

43. The method of claim 42, further comprising the step of patterning the layer of silicon-rich insulator.

44. The method of claim 42, further comprising the step of planarizing the first interlayer dielectric.

45. The method of claim 42, further comprising the step of planarizing the second interlayer dielectric.

46. The method of claim 42, wherein the steps are performed in the order recited.

47. A multilayer memory made by the method of claim 42.

48. A substrate carrying electronics comprising the multilayer memory of claim 47.

49. An integrated circuit comprising the multilayer memory of claim 47.

50. A method for fabricating a multilayer memory, the method comprising the steps of:

a) providing a substrate,

b) depositing and patterning a first conductive layer over the substrate,

c) forming a tunnel-junction layer over the first conductive layer,

d) forming a layer of silicon-rich insulator,

e) forming and patterning a first interlayer dielectric over the layer of silicon-rich insulator,

f) forming an opening through the first interlayer dielectric and extending to the layer of silicon-rich insulator,

g) filling the opening through the first interlayer dielectric with conductive material to form a middle electrode, at least a portion of the middle electrode being disposed contiguous with the silicon-rich insulator,

h) forming a storage-element layer,

i) forming and patterning a second conductive layer over the storage-element layer and at least partially aligned with the middle electrode,

j) forming and patterning a second interlayer dielectric, whereby a substrate is formed for subsequent layers,

k) forming vias as required through the second interlayer dielectric, and

l) repeating steps b) through k) until a desired number of memory array layers have been formed.

51. The method of claim 50, further comprising the step of patterning the layer of silicon-rich insulator.

52. The method of claim 50, further comprising the step of planarizing the first interlayer dielectric.

53. The method of claim 50, further comprising the step of planarizing the second interlayer dielectric.

54. The method of claim 50, wherein the steps are performed in the order recited.

55. A multilayer memory made by the method of claim 50.

56. A substrate carrying electronics comprising the multilayer memory of claim 55.

57. An integrated circuit comprising the multilayer memory of claim 55.